A 200 GHz Broadband, Fixed-Tuned, Planar Doubler

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Abstract - A 100/200 GHz planar balanced frequency doubler has been designed and tested. The doubler is designed for high output power and efficiency over a wide bandwidth without relying on mechanical tuners of any kind. The only available tuning mechanism is through an external electronic DC bias supply. The doubler employs a six anode planar Schottky Barrier varactor array fabricated at the University of Virginia Semiconductor Device Laboratory.

INTRODUCTION

The multiplier was designed as part of a local oscillator (LO) chain for the European Space Agency's (ESA) Far Infrared and Submillimeter Telescope (FIRST). Instruments on FIRST will require LO sources in seven bands covering a large part of the spectrum between 480 GHz and 2.7 THz. Since the instruments must be space qualified, the LO sources should be solid state, rugged, reliable, efficient and low noise.

The 100/200 GHz doubler described here was designed as part of an LO multiplier chain for Band 5 which covers the spectrum from 1.12-1.25 THz. It is estimated that approximately 50 μW is needed at these frequencies to pump either an SIS mixer or an HEB. Much less power is actually required by the mixers, but there are substantial optical coupling losses associated with the cryogenic dewars. The table below shows the makeup of the LO chain for Band 5. The estimated multiplication efficiencies are for room temperature operation. However, the LO chains on FIRST may be cooled to 80 K which will result in a significant increase in the multiplication efficiencies and output powers.

Table 1. Proposed LO chain for Band 5 on FIRST.

Input frequency/power	Component	Estimated efficiency	Output frequency/power
100 GHz /	MMIC amp		100 GHz / 200^{+} mW
100 GHz / 170 mW	Doubler	30 %	200 GHz / 50 mW
200 GHz / 50 mW	Doubler	14 %	400 GHz / 7 mW
400 GHz / 7 mW	Tripler	0.7 %	1.2 THz / 50 μW

SCHOTTKY BARRIER VARACTOR

The nonlinear device used in the 100/200 GHz frequency doubler is a GaAs planar Schottky barrier varactor fabricated at the University of Virginia (UVA) Semiconductor Device Laboratory (SDL). The varactor chip comprises 6 anodes in an antiseries arrangement as shown in Fig. 1. The epitaxial doping is 2×10^{17} cm^{-3}, the reverse breakdown voltage is measured to be 9.5 V/anode at 50 μA and the series resistance is estimated to be approximately 4 Ω/anode. Three versions of the varactor chip were fabricated as specified in Table 2. The values for the anode diameter, D, the zero biased junction capacitance, C_{j0}, the input frequency embedding impedance, Z_{IN}, and the output frequency embedding impedance, Z_{OUT}, are for the individual anodes. The input power required for optimum multiplier efficiency, P_{IN}, is the total for the 6 anode chip.

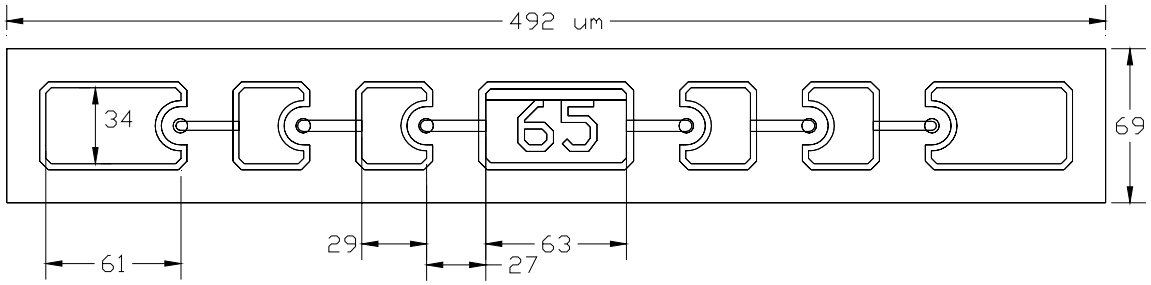

Figure 1. Sketch of the UVA planar varactor chip.

Table 2. Varactor parameters for a pump frequency of 100 GHz.

UVA type	D (μm)	C_{j0} (fF)	Z_{IN} (Ω)	Z_{OUT} (Ω)	P_{IN} (mW)
SB6T3	6.0	42	11 + j70	18 + j35	130
SB6T4	6.5	49	10 + j60	15 + j30	160
SB7T5	7.0	56	8 + j52	13 + j26	190

EMBEDDING CIRCUIT

The embedding circuit comprises a quartz circuit and varactor chip housed in a split waveguide block. This basic circuit topology can be traced back to a novel design described by Erickson in the literature [1-3]. The original architecture was later successfully modified to remove all mechanical tuners without sacrificing bandwidth [4,5]. This was achieved by mounting the planar varactor chip on a quartz circuit rather than directly across a split waveguide block. The photolithographic process used to fabricate the quartz circuits results in a high degree of control over circuit dimensions and thus significant control over the embedding impedances.

The varactors are situated in the input waveguide as illustrated in Figure 2. Input radiation is incident on the varactors in a balanced mode (TE_{10}) in reduced-height waveguide. However, the input radiation can propagate beyond the varactor chip toward the output waveguide. HFSS simulations indicate that the center conductor and quartz dielectric in this quasi-coaxial region only slightly perturb the TE_{10} mode. At a point between the varactor chip and the output waveguide, the width of the quasi-coaxial waveguide section is sufficiently reduced to cut off propagation of the TE_{10} mode, creating a reactive termination (backshort) at the input frequency. The reduced-width section, more appropriately termed as enclosed suspended microstrip, extends to the output waveguide. The position of the backshort and the length of the reduced-height waveguide section between the varactors and the full-height input waveguide are design parameters that were used to obtain an acceptable input frequency embedding impedance. The output frequency is generated by the varactors in an unbalanced mode (TEM) and is free to propagate to the output waveguide. Since the input waveguide is overmoded at the output frequency, the output radiation from the varactors can couple to the TM_{11} mode. However, this unwanted coupling can be eliminated by sufficiently reducing the input waveguide height in the region near the varactor chip.

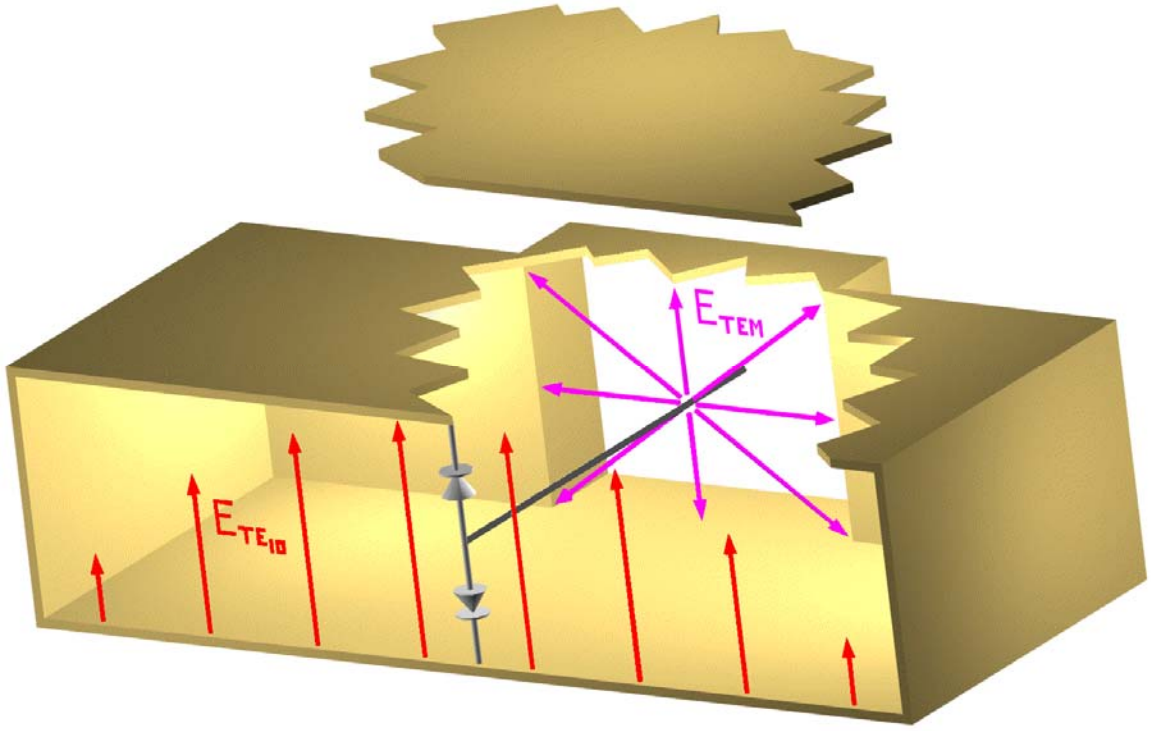

Figure 2. Conceptual sketch of the input and out electric field distributions.

A sketch of the 100/200 GHz doubler is shown in Figure 3. The input waveguide (WR-10) and output waveguide (WR-5) flanges are on opposite sides of the block and are offset by 0.3 inches. An SMA connector (not shown) is provided for DC biasing of the varactor chip. The quartz circuit sits in a groove machined in the lower half of the block. The quartz circuit comprises an output embedding circuit, a probe for a microstrip-to-waveguide transition and a low-pass hammerhead filter for an external DC bias network.

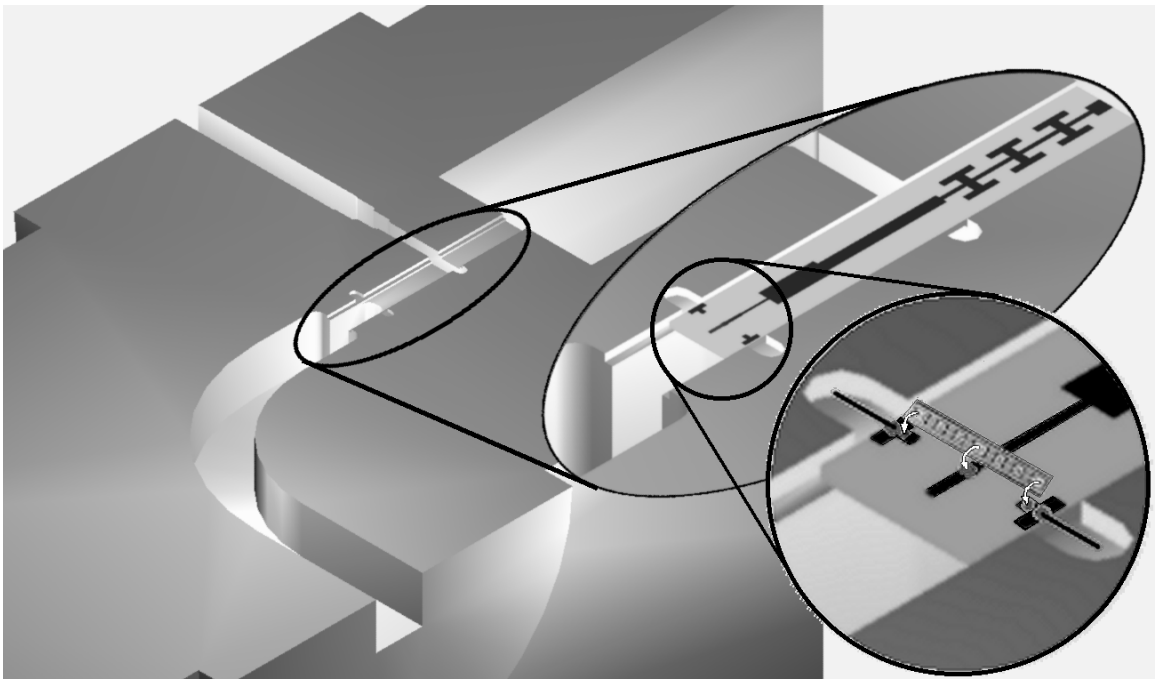

Figure 3. Sketch of the lower half of the 100/200 GHz frequency doubler block. The quartz circuit and varactor chip are shown in the magnified inserts.

The assembly process is relatively simple. First, 2 bondwires are attached to the circuit pads located at the two ends of the varactor chip and a third bondwire is attached to the large pad at the far end of the circuit beyond the hammerhead filter. The varactor chip is then soldered to 3 pads on the quartz circuit as shown in the sketch in Figure 3. The circuit is then placed in the lower half of the block, the two bondwires near the varactor chip are attached to the block and the third bondwire is attached to the center pin of the SMA connector. Finally, the two halves of the block are assembled.

EMBEDDING CIRCUIT DESIGN

The optimum embedding impedances were determined using the nonlinear analysis of Penfield and Rafuse and verified with harmonic balance simulations. The input and output embedding circuits were analyzed using Ansoft's High Frequency Structure Simulator (HFSS). Ports were attached to probes on each anode so that the individual

embedding impedances for each varactor could be monitored directly. The final HFSS simulation results are shown in the graph of Figure 4. The data for the input embedding circuit covers the frequency range from 92-106 GHz and the data for the output embedding circuit covers the frequency range from 184-212 GHz. The simulated embedding impedances are nearly optimal at the center of the bands and vary slowly with frequency. The 3 dB ouput power bandwidth of the doubler is estimated to be approximately 15 %.

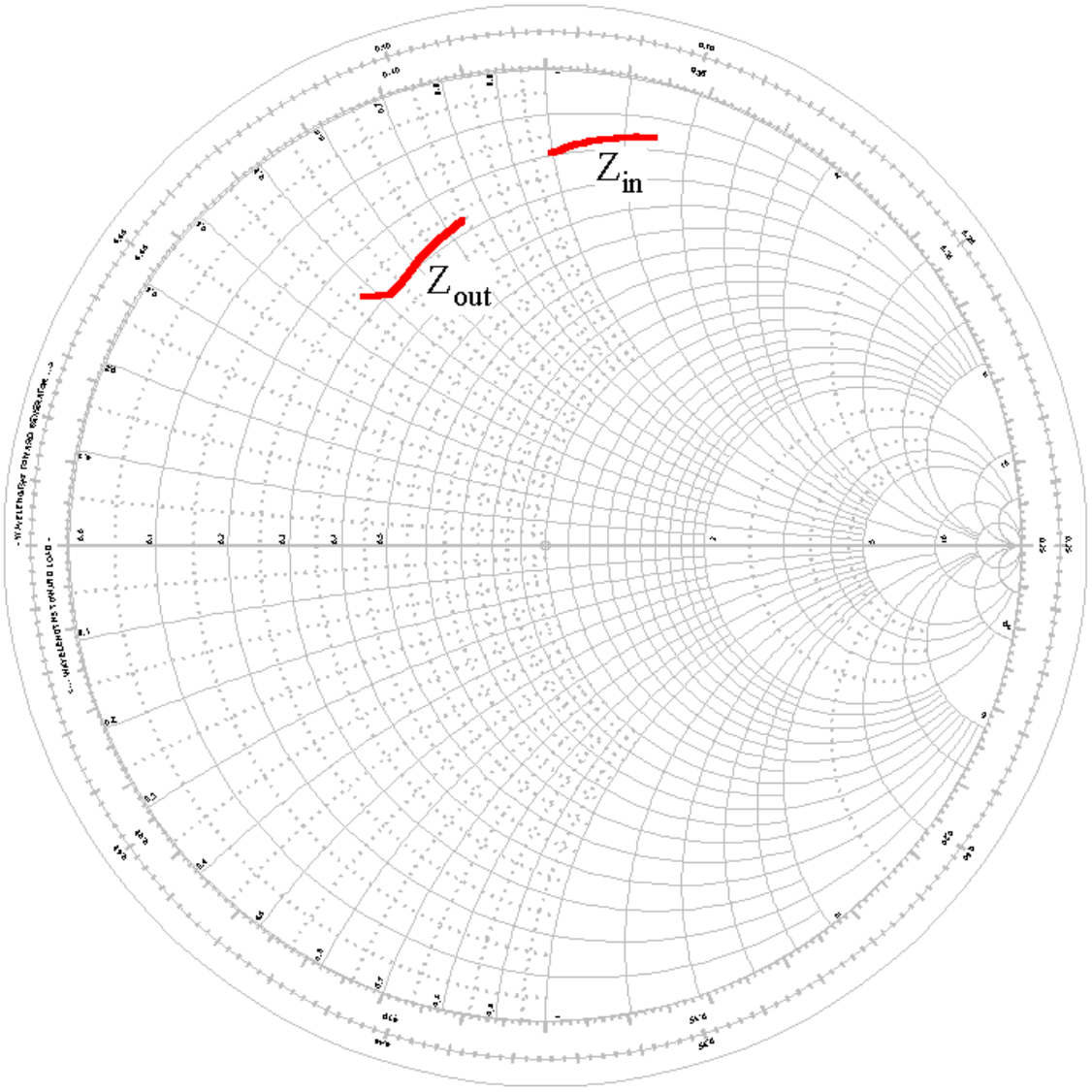

Figure 4. HFSS simulated embedding impedances.

EXPERIMENTAL RESULTS

The data shown in Figure 5 was taken at the University of Massachusetts at Amherst. Input power was provided by an IMPATT oscillator operating at 100 GHz. The varactor chip was a UVA type SB6T4 with 6.5 μm diameter anodes. The peak output power is approximately 36 mW and the corresponding efficiency is 15 %. The data was taken with the DC path open circuited so that the varactor chip was self-biased and the DC current was zero. For an available input power of 200 mW, the reflected input power was measured to be 33 mW.

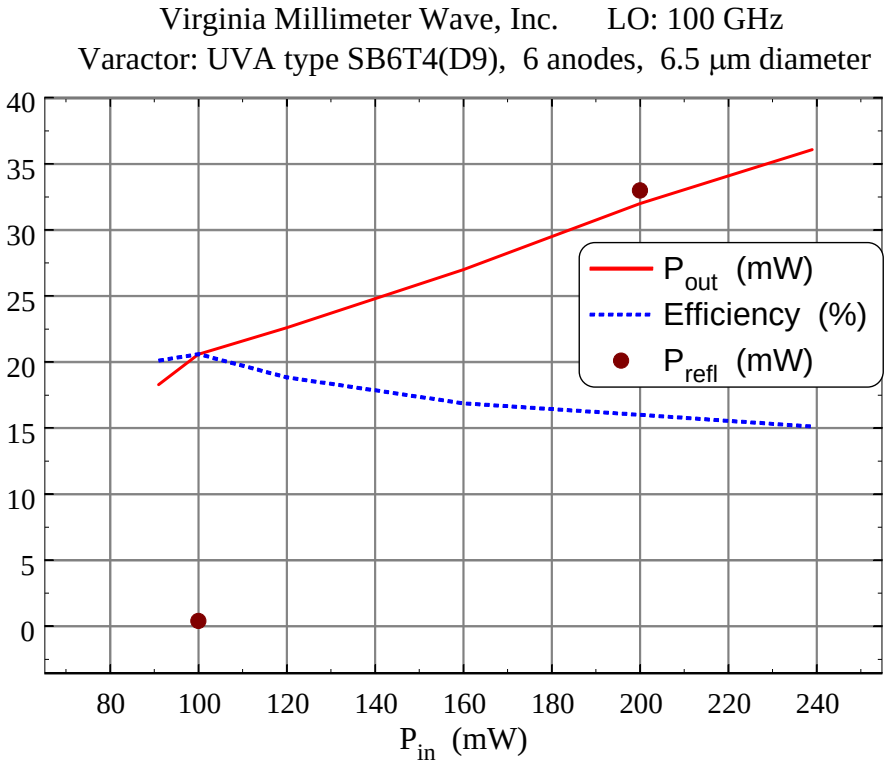

Figure 5. Measured data for the SB6T4 varactor.

Figure 6 shows measured output power and efficiency at 92/184 GHz and 100/200 GHz using a UVA type SB7T5 varactor with 7 μm diameter anodes. The data at 100/200 GHz was taken at the University of Massachusetts at Amherst using an IMPATT oscillator at 100 GHz to pump the doubler. The data at 92/184 GHz was taken at the Jet Propulsion Lab using a YIG oscillator and MMIC amplifier at 92 GHz to pump the doubler. The peak output power at 92/184 GHz was 24 mW with an input power of 148 mW and an efficiency of 17 %. The peak output power at 200 GHz was 23.5 mW with an input

power of 250 mW and an efficiency of approximately 10 %. The reflected input power for the 100/200 GHz data was measured at several points and found to be approximately 20-25 % of the available input power for pump powers above 180 mW. Peak efficiency was achieved at all points with a DC current of almost zero, indicating that the doubler was operating in an almost purely varactor mode.

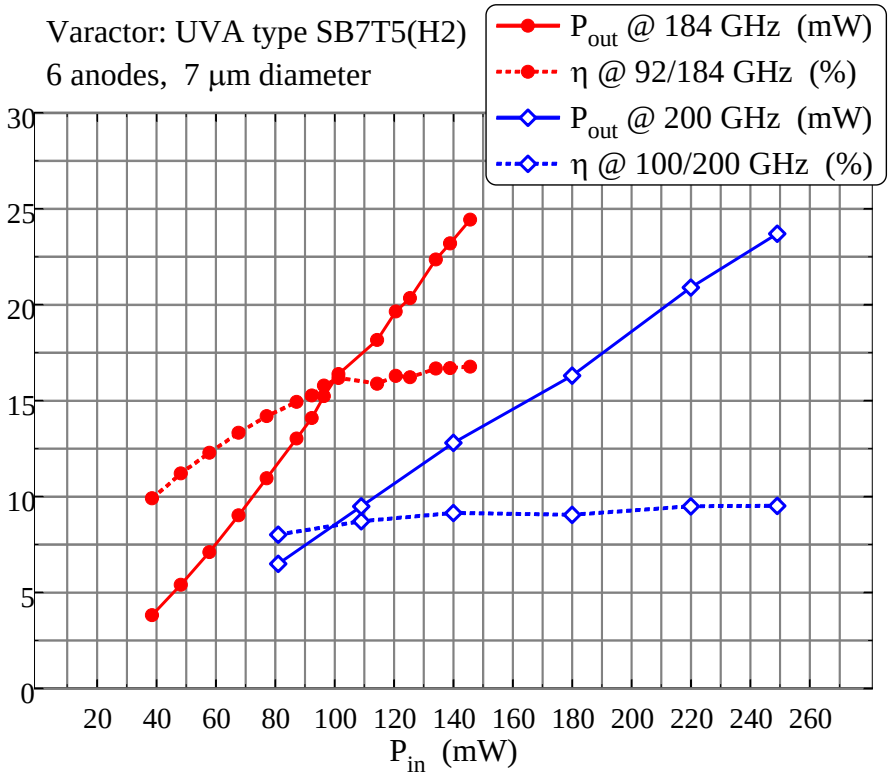

Figure 6. Measured data for the UVA type SB7T5 varactor.

The data shown in Figure 7 was taken at the University of Virginia Far-Infrared Receiver Lab in Charlottesville. Input power was provided by a commercially available Gunn effect oscillator operating over the band from 85-105 GHz. Input power levels from the Gunn ranged from a low of 35 mW at 90 GHz to a high of 95 mW at 103 GHz. The Gunn was used to drive 3 different varactor chips mounted in 3 separate blocks. The embedding circuits were identical except for small perturbations in the varactor chip and quartz circuit alignment.

Peak output power ranged from 6 mW for the SB7T5 (7 μm anodes) to 8 mW for the SB6T3 (6 μm anodes). The peak output power occurred at 96/192 GHz for all 3 varactor chips. The measured 3 dB bandwidth was approximately 9 % for the 7 μm anodes, 10 % for the 6.5 μm anodes, and 15 % for the 6 μm anodes. All 3 chips were under-pumped and thus the efficiencies were less than optimal. The increase in bandwidth for smaller anode varactors is attributable to the fact that the smaller anode varactor requires less pump power and therefore operates at higher efficiency across the band.

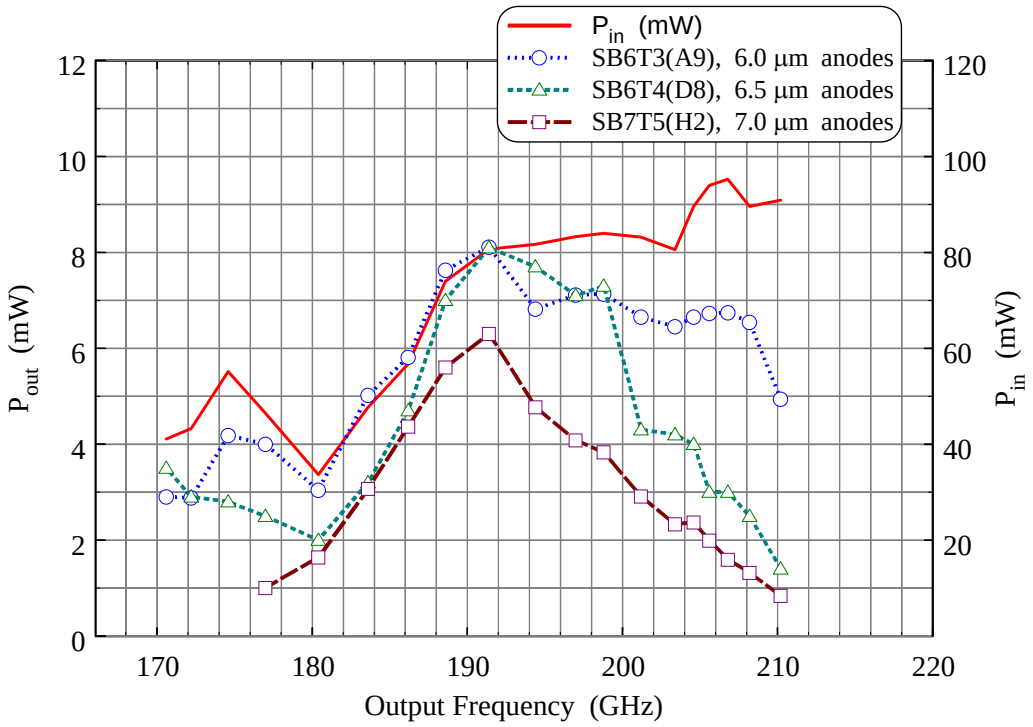

Figure 7. Measured data for 3 different varactor chips pumped with a commercially available Gunn effect oscillator.

CONCLUSION

A 100/200 GHz frequency doubler was designed and tested. The nonlinear device is a GaAs planar Schottky barrier varactor chip fabricated at the University of Virginia. The embedding circuit comprises a quartz circuit housed in a split waveguide block. The high power and large bandwidth requirements of ESA's FIRST project were the determining

factors in the design of the 100/200 GHz doubler. For optimal efficiency, the doubler requires 170 mW pump power across the band from 92-106 GHz. The source for this input drive is proposed to be a MMIC amplifier currently under development at the Jet Propulsion Lab. Since the amplifier was unavailable at the time of this report, it was impossible to fully test the multiplier. However, other high power sources were found at 92 GHz and 100 GHz and these sources were used to partially test the device.

The peak measured output power was 36 mW at 200 GHz with an input power of almost 250 mW provided by an IMPATT oscillator at 100 GHz. The peak measured output power at 184 GHz was 24 mW with an input power of 148 mW from a MMIC amplifier and YIG oscillator operating at 92 GHz. The corresponding peak efficiency was 17 %. The bandwidth was found to be approximately 15 % at drive levels below 100 mW.

There are some known problems with the current implementation of the 100/200 GHz doubler. A 20 % machine error was found in the location of the TE_{10} backshort. This error was repeated in all four manufactured blocks and was the result of an error in the CNC code. The error in the code has been fixed and new blocks will be fabricated. There were also 2 errors in the artwork for the quartz circuit. Both errors have been corrected and new photomasks have been produced. A new batch of quartz circuits will be fabricated in the coming months.

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